AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions of listings of claims in the application.

Please amend the claims 1 and 14 as follows:

1. (Currently amended) A method of fabricating a flash memory device including an array of split gate cells, comprising ~~the steps of~~:

providing a silicon substrate having a top surface;

forming a common source region in an area of said top surface for each pair of said cells;

implanting ions into predefined areas of each said common source region;

forming floating gates associated with said cells, each said floating gate having a substantial portion thereof overlying one of said predefined areas, said predefined areas having been implanted with said ions;

forming select gates each having a first extremity extending over at least a portion of one of said floating gates; and

forming drain regions associated with said cells, each said drain region being positioned proximate a second extremity of one of said select gates;

whereby said step of implanting ions into each of said predefined areas adjusts the channel threshold voltage and provides a high coupling ratio for the associated flash cell.

2. (Previously presented) A method of fabricating a flash memory device as recited in claim 1, wherein said step of forming a common source region on said substrate includes the steps of:

patterning a photoresist disposed over said substrate to substantially define said predefined area at which the common source region is to be formed;

implanting ions into said substrate to form said common source region using said patterned photoresist as an implant mask; and

removing said patterned photoresist.

3. (Previously presented) A method of fabricating a flash memory device as recited in claim 2, wherein said ions implanted to form said common source region include arsenic ions.

4. (Previously presented) A method of fabricating a flash memory device as recited in claim 1, wherein said step of forming a common source region includes the steps of:

forming a sacrificial oxide layer over said top surface of said substrate;

patterning a photoresist disposed over said substrate to substantially define said predefined area at which the common source region is to be formed;

implanting ions into said substrate to form said common source region using said patterned photoresist as an implant mask; and

removing said patterned photoresist and said sacrificial oxide layer.

5. (Previously presented) A method of fabricating a flash memory device as recited in claim 1, wherein said step of forming floating gates includes the steps of:

forming a tunneling oxide layer over each said top surface area of said substrate;

depositing a first polysilicon layer over said tunneling oxide layer;

depositing a nitride masking layer over said first polysilicon layer;

patterning and etching said nitride masking layer to expose first and second portions of said first polysilicon layer, said exposed first and second portions substantially define first and second floating gate regions;

implanting ions into said first and second floating gate regions to adjust said threshold voltage;

forming a floating gate oxide layer over said first and second exposed portions of said first polysilicon layer;

removing said nitride masking layer;

etching said first polysilicon layer and said tunneling oxide layer using said floating gate oxide layer as a mask leaving remaining portions of said first polysilicon layer and said tunneling oxide layer disposed beneath said floating gate oxide

layer, and exposing a portion of said substrate, said remaining portions of said first polysilicon layer forming first and second floating gates associated with each said cell, said floating gates having side walls and a portion which overlies a portion of said common source region thereby providing a high coupling ration for the associated cell.

6. (Previously presented) A method of fabricating a flash memory device as recited in claim 1 wherein said step of forming said select gates includes the steps of:

forming an insulating layer over the exposed portion of said substrate and the floating gate oxide layer covering said floating gates;

forming a second polysilicon layer over said insulating layer;

forming a conductive layer over said second polysilicon layer; and

removing portions of said conductive layer, said second polysilicon layer, and said insulating layer to form said select gates.

7. (Previously presented) A method of fabricating a flash memory device as recited in claim 6, wherein said step of forming an insulating layer over said exposed portion of said substrate and said floating gate oxide layer covering said floating gates includes the steps of:

forming a first gate oxide layer over said exposed portion of said substrate, over said floating gate oxide layer, and over said floating gates;

forming a nitride layer over said first oxide layer;

performing an etching process to remove a portion of said nitride layer and leaving nitride spacers adjacent said side walls of each of said floating gates; and

forming a second gate oxide layer over said first oxide layer, over said nitride spacers and over said floating gate oxide layer.

8. (Original) A method of fabricating a flash memory device as recited in claim 6, wherein said conductive layer includes tungsten.

9. (Original) a method of fabricating a flash memory device as recited in claim 1, wherein said ions include Boron ions.

10. (Previously presented) A method of fabricating a flash memory device as recited in claim 6, wherein said step of forming drain regions associated with each cell includes the steps of:

patterning and etching said conductive layer and portions of said substrate to substantially define the boundaries of drain areas of said substrate; and

implanting ions into said drain areas to form said drain regions.

11. (Currently amended) A method of fabricating a flash memory device as recited in claim 4, wherein said step of implanting said ions into said substrate to form said common source region includes:

implanting arsenic ions at a dose in the range of 1 x 10^{14} /cm^2 to 5 x 10^{14}/cm^2 ~~to provide a dopant density in the range of 1 x 1014 /cm2 to 5 x 1014/cm2~~ and at an energy range of 80 to 150 KeV.

12. (Previously presented) A method of fabricating a flash memory device as recited in claim 5, wherein said step of depositing a first polysilicon layer over said tunneling oxide layer includes:

depositing polysilicon upon said tunneling oxide at a temperature of approximately 620 degrees C in order to form said first layer having a thickness in the range of 500 to 2500 angstroms.

13. (Previously presented) A method of fabricating a flash memory device as recited in claim 12, wherein said first polysilicon layer includes SiH4.

14. (Currently amended) A method of fabricating a flash memory device having a high coupling ratio, comprising ~~the steps of~~ :

providing a silicon substrate having a top surface;

forming a sacrificial oxide layer over said top surface of said substrate;

patterning a photoresist layer disposed over said sacrificial oxide layer to substantially define a source region of the substrate;

implanting first ions into said substrate to form a common source region of said substrate using the patterned photoresist layer as an implant mask;

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removing said patterned photoresist layer and said sacrificial oxide layer to expose said top surface of said substrate;

forming a tunneling oxide layer over the exposed top surface of said substrate;

depositing a first polysilicon layer over said tunneling oxide layer;

depositing a nitride masking layer over said first polysilicon layer;

patterning and etching said nitride masking layer to expose at least one first portion and at least one second portion of said first polysilicon layer, said first and second exposed portions substantially defining first and second floating gate regions, each said floating gate region having a substantial portion thereof overlying said common source region, said common source region having a portion that has been implanted with said first ions;

implanting second ions into portions of said substrate defined by said first and second floating gate regions and including opposite extremities of said common source region, in order to adjust the threshold voltage of the flash memory device;

forming a floating gate oxide layer over said first and second exposed portions of said first polysilicon layer;

removing said nitride masking layer;

etching said first polysilicon layer and said tunneling oxide layer using said floating gate oxide layer as a mask leaving remaining portions of said first polysilicon layer and said tunneling oxide disposed beneath said floating gate oxide layer, and exposing a portion of said substrate, each said remaining portion of said first polysilicon layer forming a floating ate having side walls;

forming a first gate oxide layer over said exposed portion of said substrate, over said floating gate oxide layer, and over said floating gates;

forming a nitride layer over said first oxide layer;

performing an etching process to remove a portion of said nitride layer and leaving nitride spacers adjacent said side walls of each of said floating gates;

forming a second gate oxide layer over said first oxide layer, over said nitride spacers and over said floating gate oxide layer;

forming a second polysilicon layer over said second gate oxide layer;

forming a conductive layer over said second polysilicon layer;

removing portions of said conductive layer, said second polysilicon layer, said second gate oxide layer, said nitride spacers and said first gate oxide layer to form a plurality of select gates each having a portion overlying a portion of an associated one of said floating gates;

patterning and etching said conductive layer to expose portions of said substrate to substantially define the boundaries of at least on drain area of said substrate; and

implanting third ions into said drain area of said substrate to form at least one drain region;

whereby the floating gate having a portion which overlies a portion of said common source region thereby providing a high coupling ratio for an associated cell.

15. (Cancelled)

16. (Previously presented) A method of fabricating a flash memory device as recited in claim 14, wherein said first ions include N-type ions and said second ions include P-type ions, whereby threshold voltage of the flash memory device is adjusted.

17 – 20. (Withdrawn)